Elimination of leakage in GaN-on-diamond

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Abstract − **The use of chemical vapor deposition diamond as a substrate for gallium nitride (GaN) to form GaN-on-diamond has the potential to allow for higher linear power densities in GaN high electron mobility transistors (HEMTs). The increase in GaN HEMT power density on diamond has been limited to date by the electrical leakage in GaN-on-diamond substrates. In this paper we show that to eliminate buffer leakage in silicon based GaN-on-diamond, you have to completely remove the transition layers used to grow high quality GaN on the original host silicon. By completely removing the transition layers in GaN-on-diamond, we demonstrated buffer leakage comparable to the leakage in GaN on silicon carbide.**

Index Terms − **GaN-on-Diamond, HEMT, GaN**

I. Introduction

The introduction of chemical vapor deposition (CVD) diamond as a viable substrate for GaN HEMTs [1], [2] makes it attractive to run higher power densities through the GaN HEMT than is normally used for traditional GaN host substrates [3]. While power densities of 20 and 40W/mm have been demonstrated for pulsed devices on silicon carbide (SiC) [4], continuous powers exceeding 10W/mm will reduce the lifetime of the GaN HEMTs due to self-heating.

GaN-on-diamond holds a promise of reducing the problems associated with self-heating and allows for increases in the power density of HEMT devices. To date, GaN-on-diamond has been shown to allow for higher areal power densities than GaN-on-SiC [5], [6].

The increase in areal power density is achieved by reducing the gate-to-gate spacing in a HEMT. While this method is a useful way to get higher power densities, it still runs into practical limits associated with via holes and metal lines with aspect ratios difficult to fabricate. Another way to increase the power density is to increase the device bias voltage. By increasing the bias voltage without changing the device design, one can get to higher power densities. One factor limiting increases in bias voltage for GaN-on-diamond has been the device leakage. As the bias is increased, the leakage current limits the shut-off of the devices.

Leakage in GaN HEMT devices can be on the GaN surface, in the GaN buffer, or at the interface between the GaN and the diamond. In this paper we investigate the sources of GaN-on-diamond leakage in the buffer and at the interface between the GaN and the diamond (for simplicity refer to the combination of buffer and interface leakage as buffer or bulk GaN leakage). The goal is to understand the sources of leakage and ultimately control the leakage, so that higher bias voltages can be used to increase the linear power density in GaN-on-diamond devices.

II. Method of Making GaN-on-Diamond

The method used to create GaN-on-diamond, (described in more detail in [7]), involves a double flip of the GaN epi, an etch of nucleation layers, and a diamond growth which exposes the GaN epi to elevated temperatures for an extended period. We have shown in the past that the resulting epi exhibits leakage at higher bias voltages on devices. It is our belief that surface currents must be controlled at the device fabrication level, buffer leakage must be controlled at the materials level. To understand buffer leakage, we fabricated test devices that removed the two-dimensional electron gas (2DEG) and isolated the surface, allowing us to focus exclusively on the leakage currents through the bulk GaN buffer. Our objective with this study was to understand the mechanisms which drive the leakage with the intention of eliminating them.

A. GaN-on-Diamond Test Devices

GaN-on-diamond test devices are made by depositing contact metals and annealing to form Ohmic contacts. Isolation channels are etched into the GaN then Schottky contacts and overlay metals are deposited. The isolation region is about 10 microns long and 100 microns wide. A cross-sectional schematic is shown in Figure 1. The voltage is applied between V_{source} and bulk pad. Any surface current is collected in the guard ring. A detailed description of the fabrication and design is found in [8]. We thermally evaluated the GaN-on-diamond material using Time Domain Thermal Reflectance [11]. The wafers had a thermal boundary resistance of 30± 3m^{2}K/GW and diamond substrate conductivity greater than 1500W/mK.

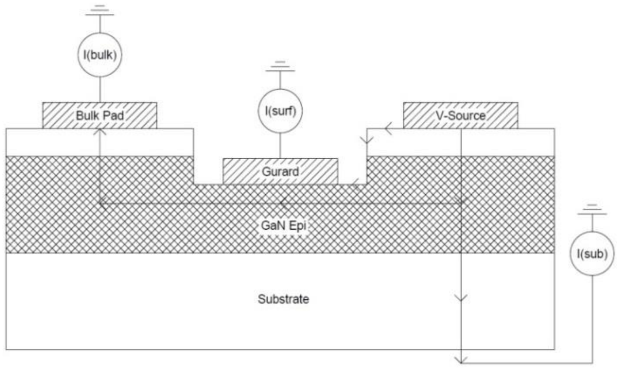


Fig. 1 Test structure used to measure buffer, surface and substrate leakage.

III. Effect of the Transition Layers

The transition or nucleation layers in GaN-on-diamond are a highly defective superlattice made up of different compositions of aluminum gallium nitride (AlGaN). As the superlattice grows, the number of defects is reduced. The problem with GaN-on-silicon is that the transition layers (TLs) have defects which have poor electrical and thermal properties. The thermal conductivity, measured at 10 W/mK [9] is reason enough for wanting to remove these layers. However, in most systems, removing the TLs is not possible because they are critical for forming high quality GaN on host substrate. In our GaN-on-diamond fabrication process we have direct access to the defective AlGaN layers so have the ability to remove them. The problem in removing the AlGaN layers is that the high level of defects also leads to non-uniform etching which can mean incomplete removal of the AlGaN. With the TLs removed, multiple teams have fabricated devices on our material and demonstrated that the thermal properties of the GaN-on-diamond exceed that of GaN-on-silicon carbide [5],[6].

In addition to the poor thermal conductivity, the electrical properties of the TLs are also undesirable, as grown on silicon the AlGaN transition layers are highly defective and often dope the silicon, creating a back barrier which impairs the performance of both GaN power and GaN HEMT devices. When we make GaN-on-diamond we remove the TLs eliminating many of the problems associated with the AlGaN, however this process creates a new interface in the system which needs to be understood.

Here we compare the electrical properties of GaN-on-diamond to those of GaN on silicon and on silicon carbide as a way to understand the electrical properties of the interface between the GaN and the diamond as well as the properties of the GaN buffer which has been exposed epi flip and diamond synthesis process. We test the GaN buffer and interface on devices and un-processed wafers.

IV. Fabrication and Measurements

We fabricated GaN devices on each of the host substrates (diamond, silicon and silicon carbide) as seen in figure 1. For devices we look at the buffer leakage. Again, we consider as buffer leakage the current flowing through the buffer and possibly along the interface between the GaN and the diamond given that we can't isolate these two current paths. The device level buffer GaN leakage current measurements are made on devices with the 2DEG eliminated and the surface currents collected. By eliminating the 2DEG and capturing the surface currents, the current flow measured is only in the buffer GaN.

We chose not to investigate the surface leakage currents because each device manufacturer who uses our GaN-on-diamond wafer will have a slightly different surface condition and will need to work out surface passivation separately. However, buffer leakage currents are a materials problem which would be much harder to solve at the device level. Here we seek to characterize the quality of the buffer GaN and compare it to the buffer GaN grown on SiC without having been transferred to diamond.

Our critical parameter on wafer level measurements is the flat band capacitance in mercury probe capacitance voltage (CV) left after the 2DEG has been depleted [10]. We typically make the wafer level measurements with the GaN surface passivated with 500 angstroms of silicon nitride. The surface passivation allows us to isolate the buffer characteristics without having the surface currents affect our measurements. In the CV measurements, we deplete the GaN up to 30V to investigate the charges well into the host substrate.

If the GaN buffer has been damaged during the epi transfer process, we expect to see greater leakage currents on devices and higher residual capacitance on mercury probe measurements. Possible damage mechanisms include: exposure to temperature during diamond synthesis, exposure of the nitrogen face GaN during the TL etch, residual damage left after the removal of the AlGaN TLs or possibly bending induced strain due to the difference in expansion coefficient between the silicon and the diamond.

IV. Results and Discussion

A. Device Measurements

Fig. 2 shows measurements of 6 devices on one wafer. The leakage in all cases stays below 10µA/mm at 30V. This corresponds to a bulk resistance of approximately 10MΩ which is equivalent to a resistivity of 10KΩ·cm. However we notice that there is a binomial distribution in the leakage plots. Some devices have leakage of less than 10nA others have leakage close to 1μA @ 30V bias. This distribution of results points to a localized leakage phenomena.

We used emission microscopy (EMMI) and optical-beam induced resistance change (OBIRCH) microscopy to identify where the leakage spots in both low leakage and high leakage devices on this wafer. Low leakage devices (Fig. 3a and b) showed no specific leakage spots when compared to the background and noise levels. The high leakage devices (Fig. 3c and d) showed specific leakage spots in both EMMI and OBIRCH techniques; leakage spots were identical in location with both techniques. We cross-sectioned a high leakage device using a focused ion beam etcher (FIB) to identify the cause of the leakage. The leakage spot and can be seen in Fig. 4a. The defect we found was a remnant of the TLs that were not etched during the TL removal. Fig. 4b shows an example of what

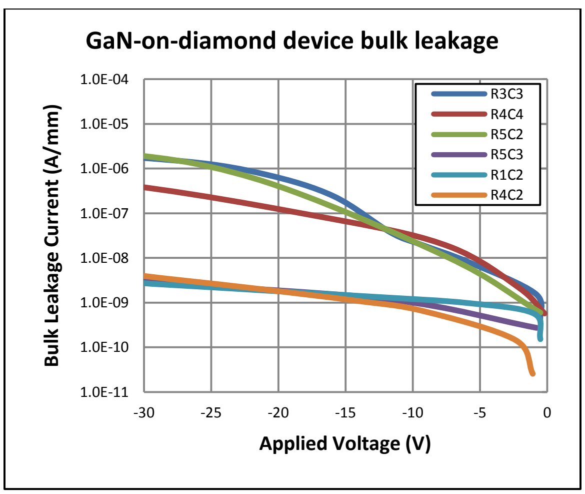


Fig. 2 Leakage measurements for various devices across an older generation GaN-on-diamond wafer.

this residue looks like before diamond growth. Previous etch techniques left this residue, which lead to a larger leakage current (Figure 3a). We found that carefully removing all the TLs results in lower leakage current. The lower leakage results are noticeable at wafer level CV measurement.

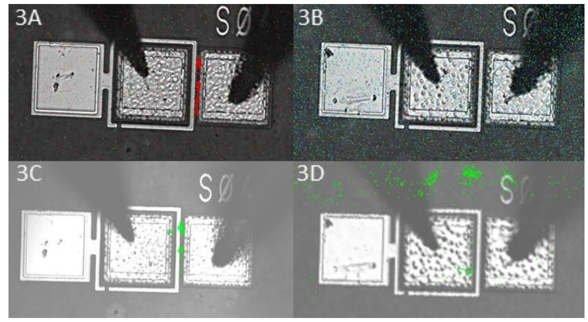


Fig. 3 a) An EMMI image of a high leakage device and b) an EMMI of a low leakage device c) an OBIRCH of the same high leakage device and d) OBIRCH of the same low leakage device.

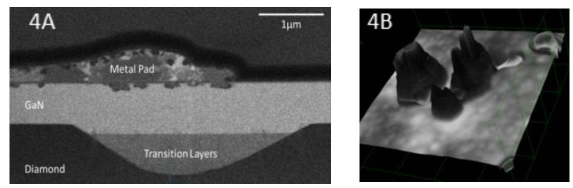
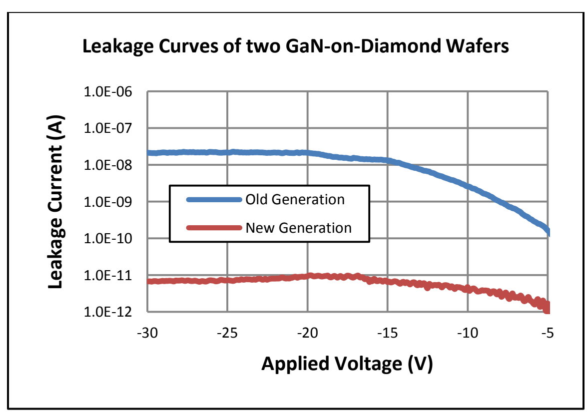


Fig. 4 a) FIB cross-section of device in figure 3a and b) laser confocal microscope image showing post transition etch residue prior to diamond deposition on a separate wafer.

B. Wafer Level CV Measurements

The mercury probe capacitance-voltage (CV) measurements of the AlGaN/GaN HEMT structures allow us to assess the quality of the GaN buffer and interface material. Figure 5 compares two versions of GaN-on-diamond before and after we optimized the AlGaN etch. The flat band capacitance (capacitance at high reverse bias) is indicative of GaN buffer and interface charge/doping seen in Fig. 5b [10].



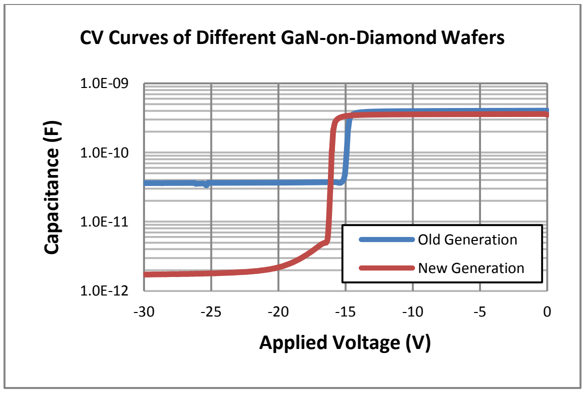


Fig. 5 a) Mercury probe CV of a wafer with residue (Old Generation) and a wafer without residue (New Generation). b) Mercury probe leakage of a wafer with residue (Old) and a wafer without residue (New).

GaN-on-diamond material with no residue has a flat band capacitance of approximately 2.5pF and current leakage orders of magnitude lower than older generation GaN-on-diamond; this capacitance is similar to the value measured on as-grown GaN-on-SiC material (Table 1) and far lower than what is measured on GaN-on-silicon (approximately 18pF).

Wafer Type	# of Samples	Average Flat Band Capacitance (pF)	Standard Deviation (pF)
GaN-on-Diamond	17	2.54	1.5
GaN-on-Si	10	17.8	0.13
GaN-on-SiC	1	1.91	N/A

Table 1 Flat Band Capacitances of Various Wafers Measured from Mercury Probe CV.

Conclusions

Mercury probe CV and device measurements show that the transition layers from GaN-on-silicon to GaN-on-diamond must be removed to ensure low flat band capacitance and low leakage current. As the defective transition layers are removed, the electrical properties of the GaN-on-diamond material are comparable to that of GaN-on-SiC and an improvement compared GaN on its original host silicon.

References

[1] J.G. Felbinger, M.V.S. Chandra, Y. Sun, L.F. Eastman, J. Wasserbauer, F. Faili, D. Babic, D. Francis, and F. Ejeckam, "Comparison of GaN HEMTs on diamond and SiC substrates," Electron Device Letters, IEEE 28 (11), 2007, 948-950; B)

[2] J. Felbinger, M. V. S. Chandra, Y. Sun, L. F. Eastman, F. Ejeckam, D. Francis and J. Wasserbauer "Fabrication & Characterization of GaN-on-Diamond HEMTs" presented at WOCSEMMAD, Feb 18-22, 2007, Savannah, GA

[3] Microsemi PPG, "Gallium Nitride (GaN) versus Silicon Carbide (SiC) In The High Frequency (RF) and Power Switching Applications," www.Digikey.com

[4] Wu, Y. F., Moore, M., Saxler, A., Wisleder, T., & Parikh, P. (2006, June). 40-W/mm double field-plated GaN HEMTs. In Device Research Conference, 2006 64th (pp. 151-152). IEEE.

[5] D. Altman, M. Tyhach, J. McClymonds, S. Kim, S Graham, J. Cho, K. Goodson, D. Francis, F. Faili, F. Ejeckam, and S. Bernstein, "Analysis and Characterization of Thermal Transport in GaN HEMTs on Diamond Substrates", submitted to I-THERM 2014 Conference in Orlando, FL.

[6] D.C. Dumka, T.M. Chou, D. Francis, F. Faili, and F. Ejeckam, "AlGaN/GaN HEMTs on Diamond Substrate with over 7 W/mm Output Power Density at 10GHz", accepted to IEEE Electronics Letters (Issue #20, 2013).

[7] F. Ejeckam, D. Francis, F. Faili, F. Lowe, D. Twitchen, and B. Bolliger, "GaN-on-Diamond Wafers: A Progress Report" in GOMACTech-14 Conference, Mar 31 – Apr 3, Charleston, S.C. Results recently submitted to IMAPS (Oct 14-16, 2014, San Diego, CA) by Prof. Grace Xing of Notre Dame University.

[8] Tan, W.S., Uren, M.J., Houston, P.A., Green, R.T., Balmer, R.S. and Martin, T., 2006. Surface leakage currents in SiN x passivated AlGaN/GaN HFETs. Electron Device Letters, IEEE, 27(1), pp.1-3.

[9] Cho, Jungwan, et al. "Improved thermal interfaces of GaN–diamond composite substrates for HEMT Applications." Components, Packaging and Manufacturing Technology, IEEE Transactions on 3.1 (2013): 79-85.

[10] Mishra, U.K., Shen, L., Kazior, T.E. and Wu, Y.F., 2008. GaN-based RF power devices and amplifiers. Proceedings of the IEEE, 96(2), pp.287-305.

[11] Pomeroy, J. W., Simon, R. B., Sun, H., Francis, D., Faili, F., Twitchen, D. J., & Kuball, M. (2014). Contactless Thermal Boundary Resistance Measurement of GaN-on-Diamond Wafers. Electron Device Letters, IEEE, 35(10), 1007-1009.