Achieving the Best Thermal Performance for GaN-on-Diamond

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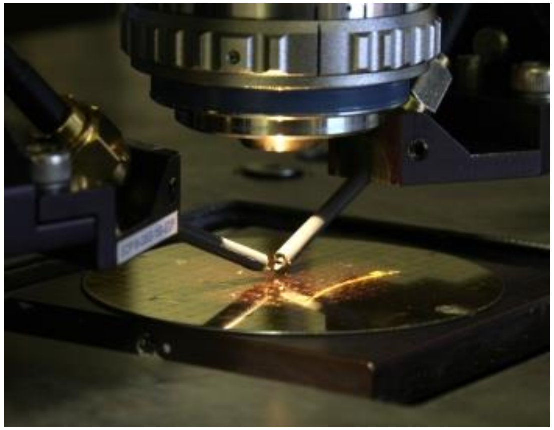
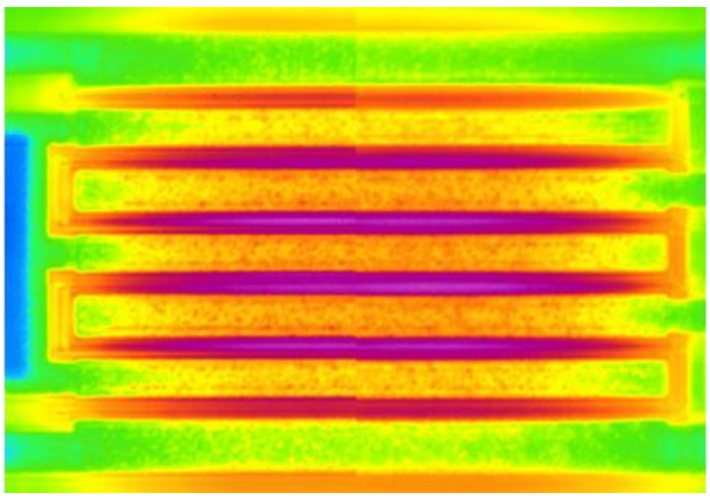
Outline

- Aim: **Optimize thermal resistance in GaN-on-Diamond through measurement and modelling**
- Review state-of-the-art GaN-on-Diamond transistor versus GaN-on-SiC
- Novel thermal resistance measurement:
  - Substrate thermal conductivity
  - Interfacial thermal resistance
- Validated transistor model for identifying thermal bottle necks in GaN-on-Diamond
- Summary

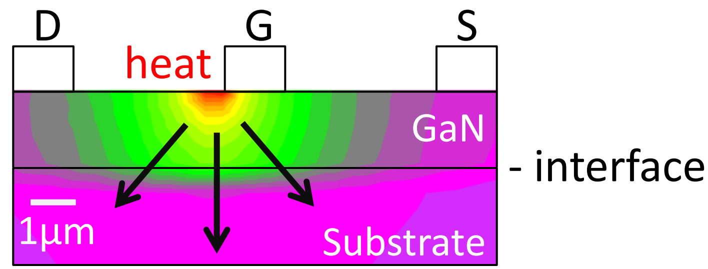


Motivation

High RF output power density in GaN-based HEMTs requires improved thermal management



Multifinger GaN HEMT thermal image



Thermal resistances near the HEMT channel:

GaN epilayer

+ GaN/substrate interface

+ Substrate

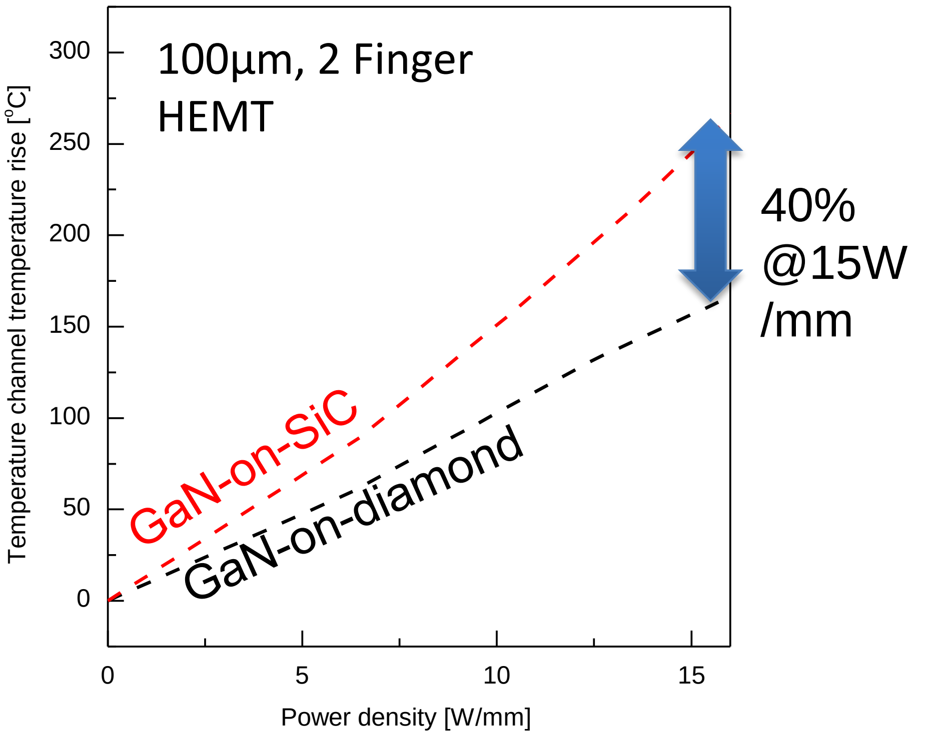
Thermal conductivity can be improved up to 5×, replacing SiC->diamond

Review: GaN-on-Diamond State-of-the-art

- Advantage over GaN-on-SiC already demonstrated: 10.8°Cmm/W (D.C. Dumka, F.4 CSICS 2013)

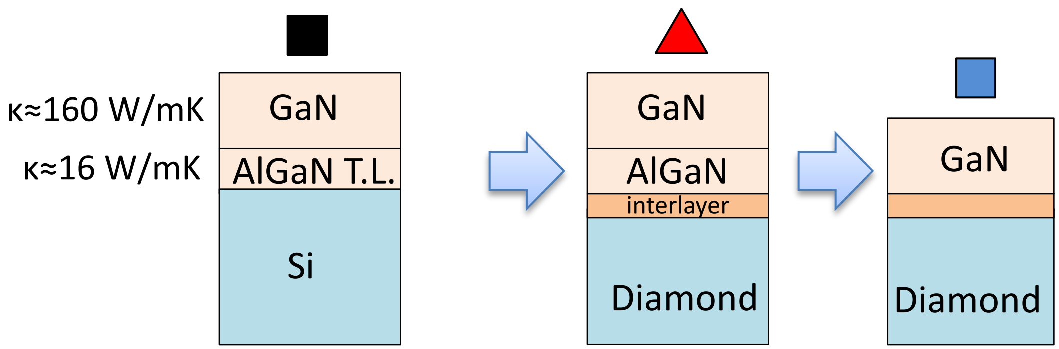
- How can we improve GaN-on-Diamond even further?

Peak channel temperature derived from Raman measurement



Historical Development

Using experimental feedback to aid design

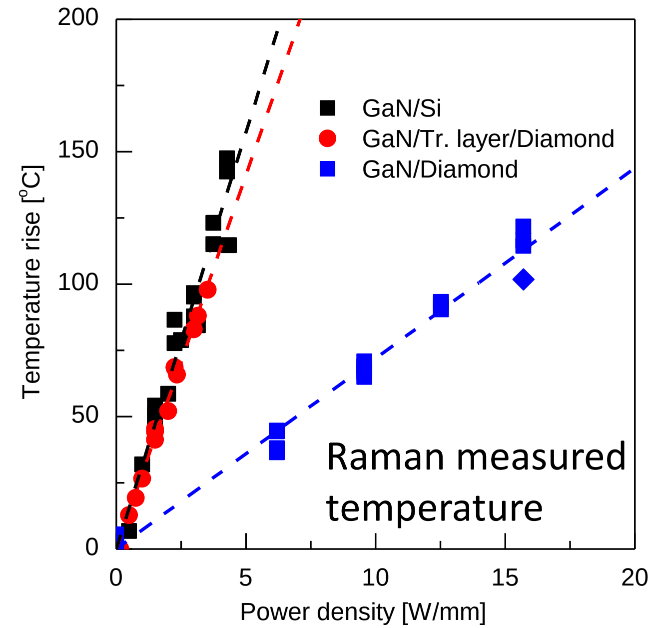


GaN transistors originate from GaN-on-Si growth

GaN-on-diamond Including transition layer

Current design, T.L. removed

2x100µm HEMT comparison

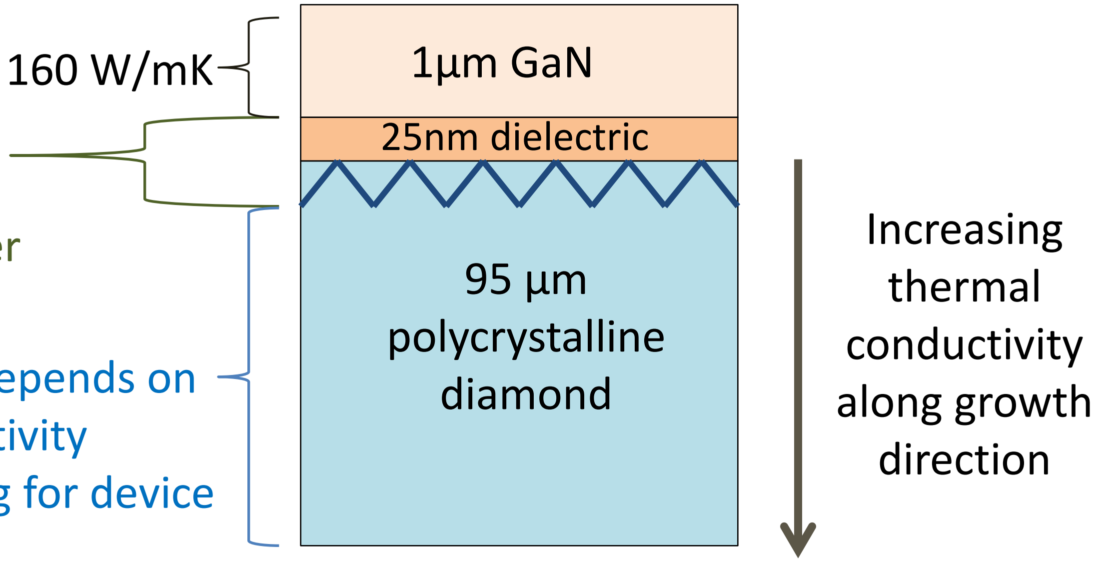


Lets examine thermal resistance in more detail

Thermal Resistance Components

TBR_{eff}?: Effective thermal resistance of interface region, including dielectric + diamond nucleation layer (<100 nm)

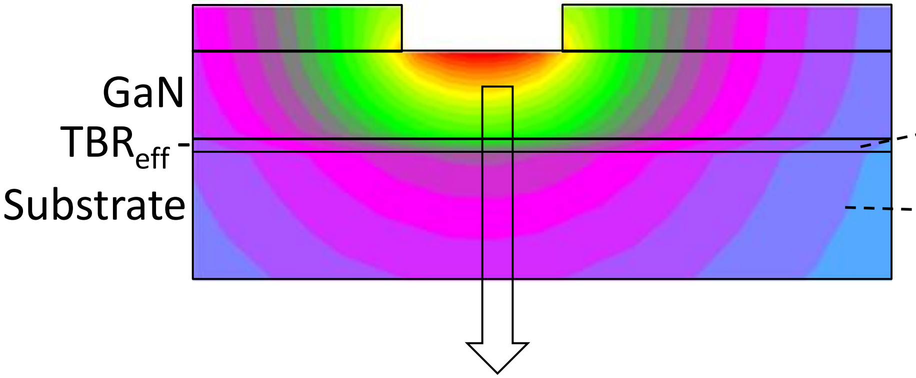
$\kappa_{diamond}$?: Thermal conductivity depends on grain size. “Bulk” thermal conductivity measurements may be misleading for device modelling



-> **Aim:** Separate these thermal resistance contributions

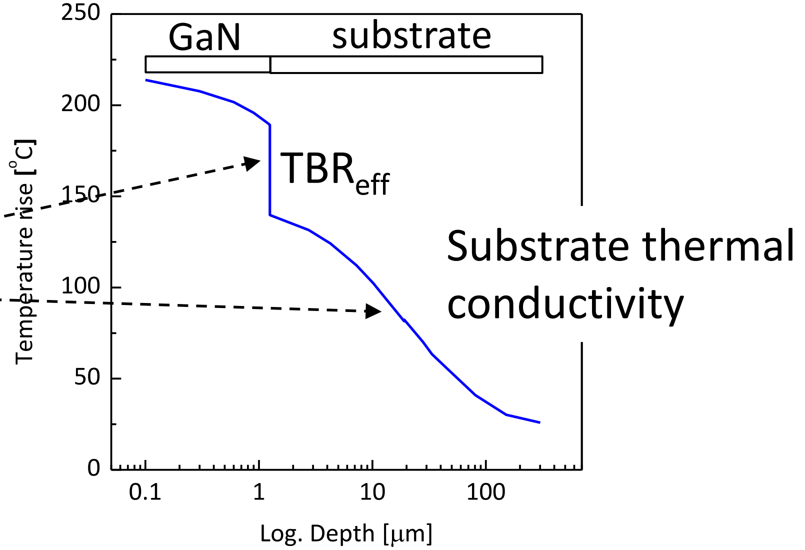
Raman Thermography Depth Mapping

Ungated transistor as a uniform heat source



Confocal depth mapping through transparent uniform materials

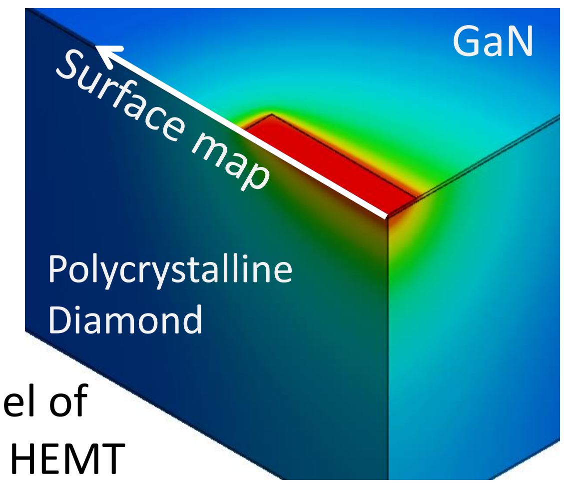
Temperature gradient->thermal parameters



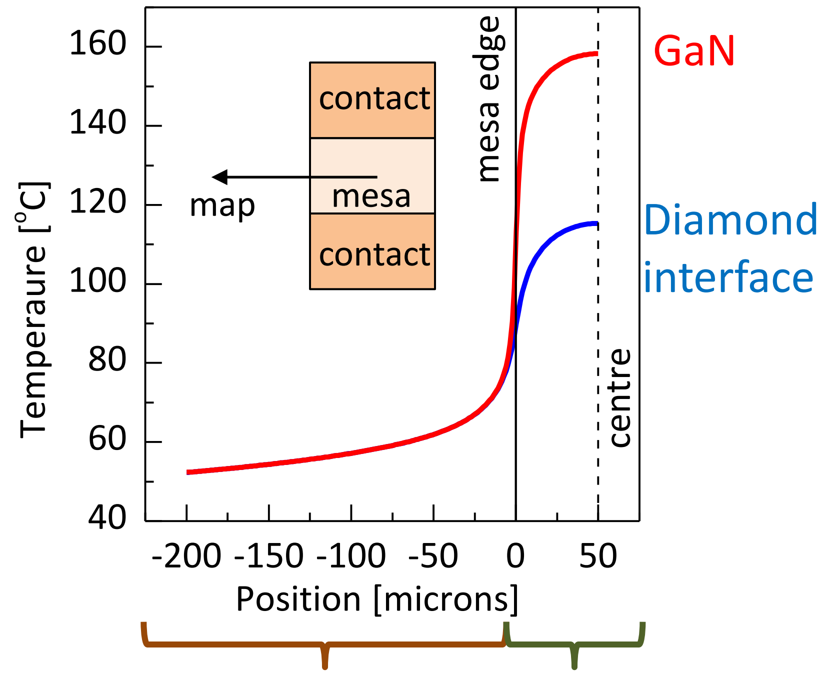
Raman temperature mapping **through** polycrystalline diamond is challenging: Light absorption and stress variation

Surface Temperature Profile

- For highest accuracy, we measure the temperature in the uniform GaN layer, rather than the diamond.



F.E. model of ungated HEMT ¼ cross section

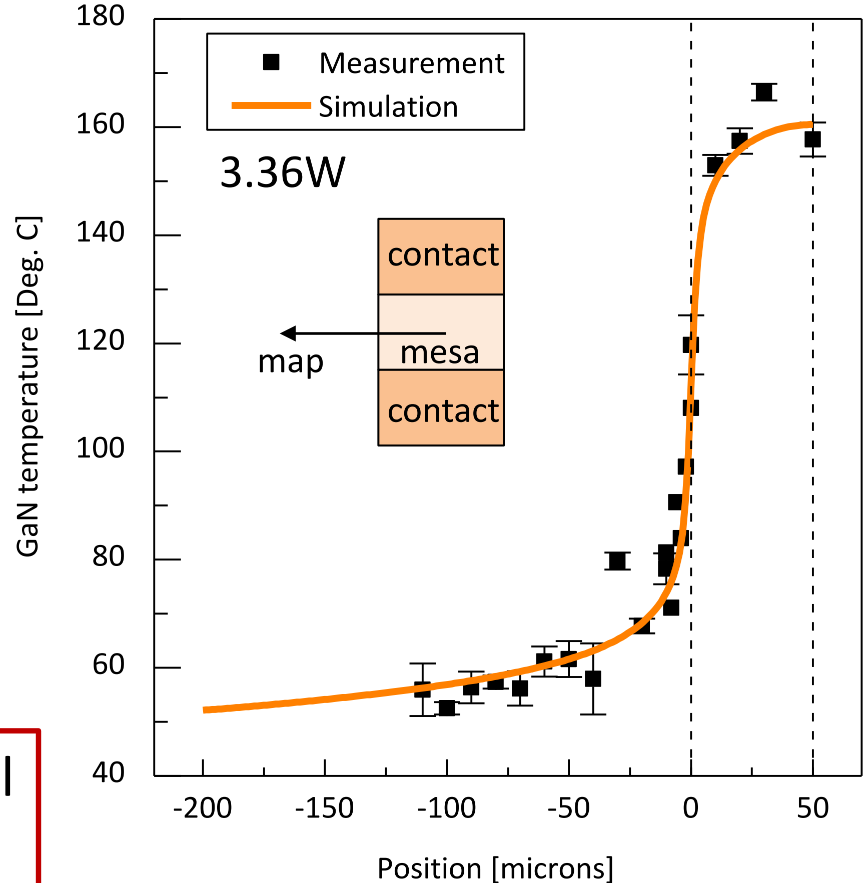


Fit finite element model by adjusting two parameters:

Diamond thermal conductivity + GaN/diamond interface TBR_{eff}

Thermal Resistance Measurement

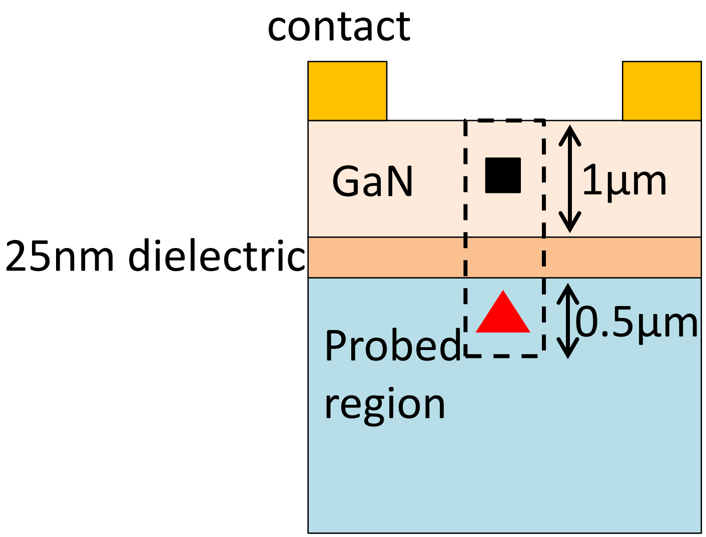
- Opaque diamond
- Effective diamond substrate thermal conductivity = 710±40 W/mK
  - 70% increase over SiC
- GaN/diamond TBR_{eff} = 2.7±0.3 $\times10^{-8}$ m^2K/W
  - Comparable to typical GaN-on-SiC TBR



Will result in lower transistor thermal resistance than GaN-on-SiC...

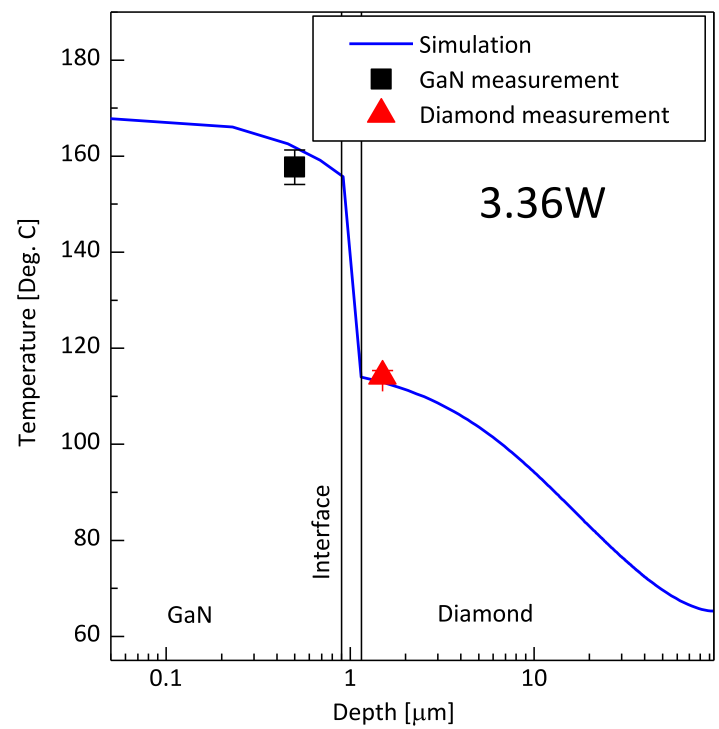
Validating Thermal Model

Measurement



Opaque diamond enables measured diamond temperature to be compared to model

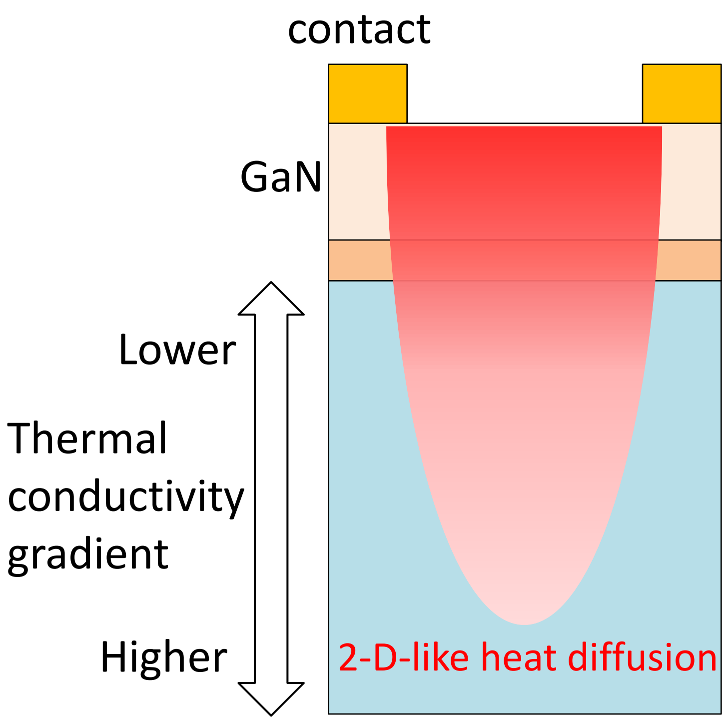
Model input parameters are fixed

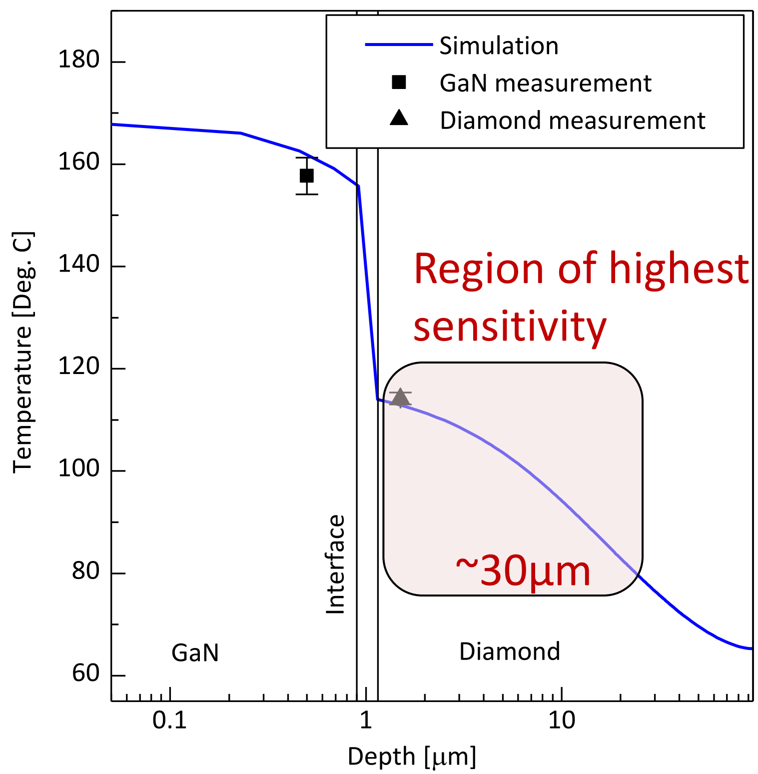


Self consistency between measurement and model

Diamond
GaN

"Effective" Substrate Thermal Conductivity

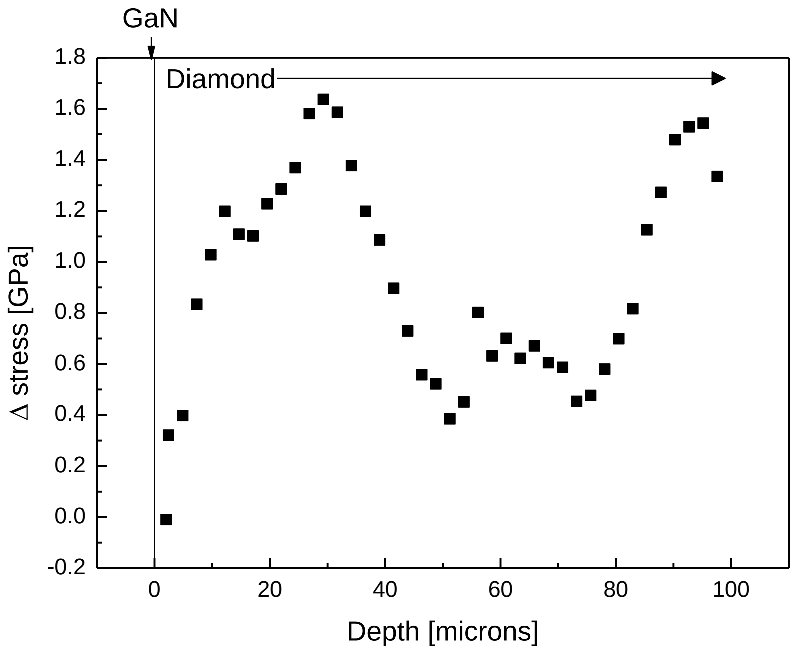




- Effective thermal conductivity < bulk thermal conductivity
- Effective thermal conductivity is relevant for transistor modelling

Wafer 2: Higher Grade Diamond

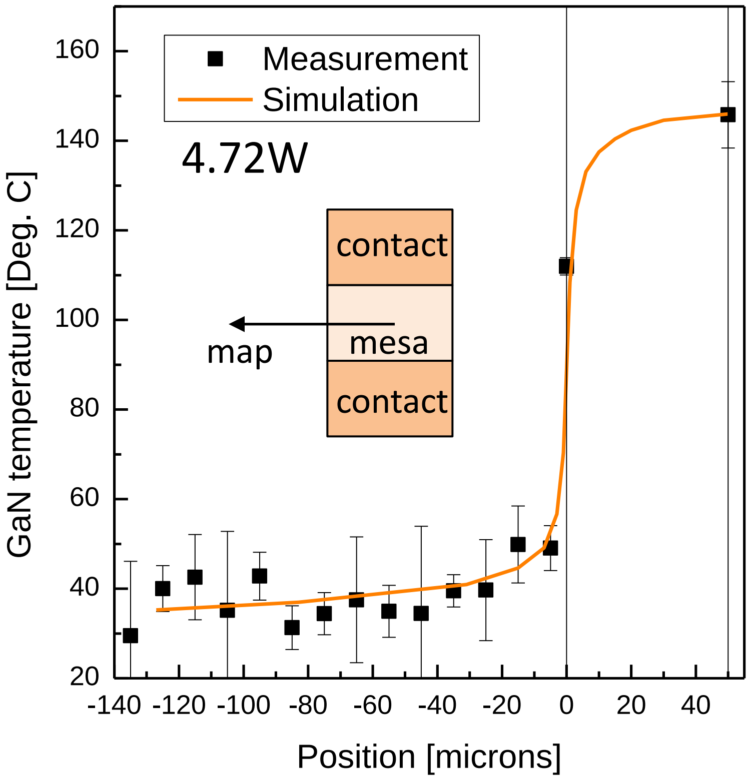
Raman temperature mapping though translucent diamond is difficult, due to stress variations



GaN surface temperature mapping approach can still be applied with high accuracy

Wafer 2: Thermal Measurement

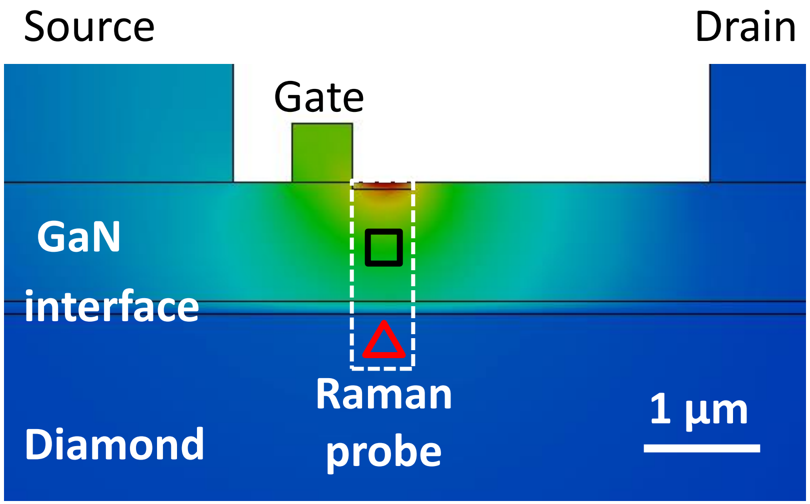
- **1200 W/mK** effective diamond thermal conductivity
- Thicker 50nm interlayer (w.r.t opaqe wafer), resulting in a 40% higher interface thermal resistance

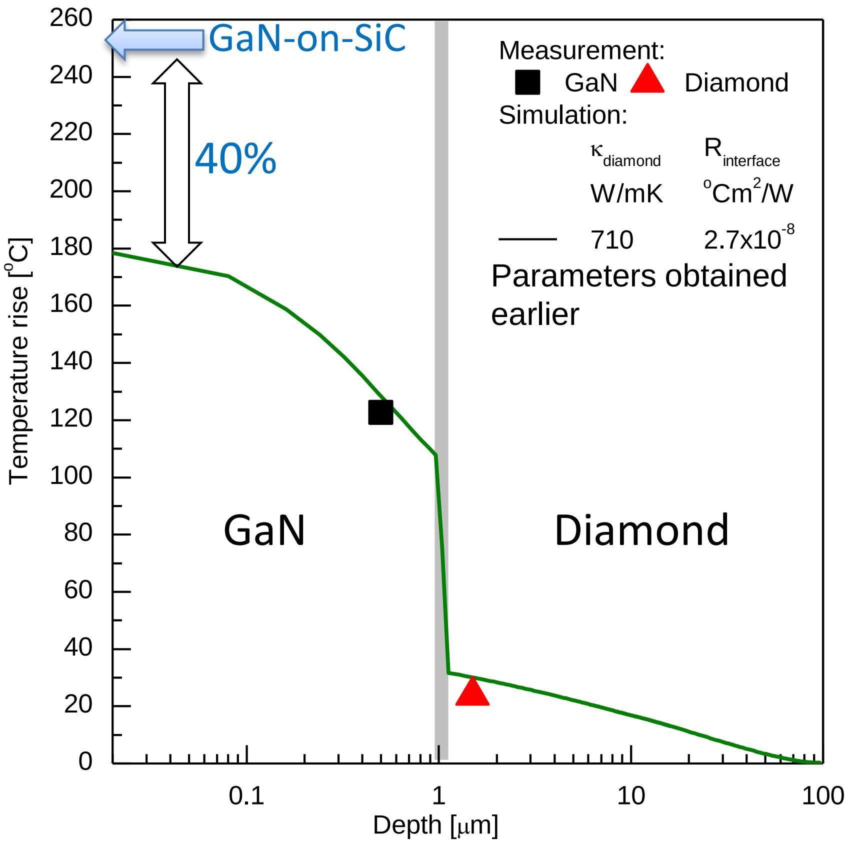


What is the relationship between interface thermal resistance, substrate thermal conductivity and transistor thermal resistance?

Transistor Thermal Model

Opaque diamond wafer, 2×100µm HEMT,
P_{diss} = 15.3 W/mm





Model validation: Agreement with measured temperatures

Reducing Transistor Thermal Resistance

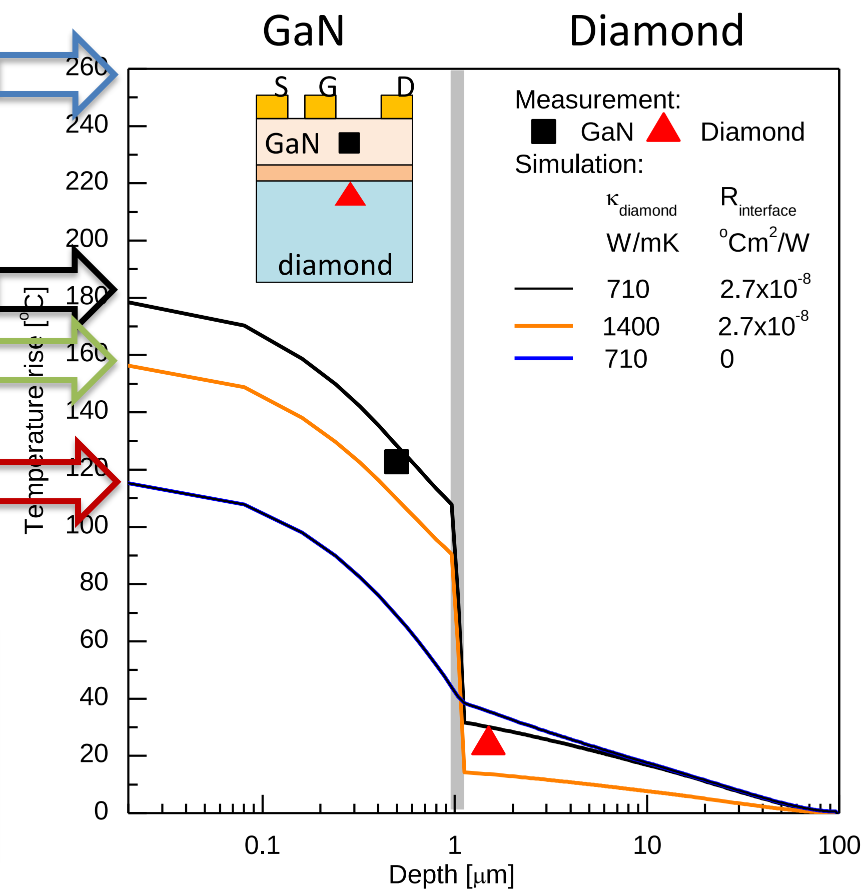
Use validated transistor model to explore thermal resistance components

GaN-on-SiC

Current GaN-on-diamond

Increasing diamond thermal conductivity

OR decreasing interface thermal resistance



Eliminating GaN/Diamond interface resistance reduces transistor thermal resistance by a further **35%**

Summary

- A 40% reduction in channel thermal resistance has been demonstrated for current GaN-on-diamond transistors versus GaN-on-SiC
- A further 35% reduction in transistor thermal resistance could be achieved by reducing the GaN/diamond interface thermal resistance
- A methodology has been developed for characterising the thermal resistance components of GaN-on-Diamond:
  - Effective diamond thermal conductivity 750-1200 W/mK
  - GaN/Diamond interfacial thermal resistance $2.7 \pm 0.3 \times 10^{-8}$ m^2K/W for 25 nm interlayer

Acknowledgement: This work is supported by the DARPA Near Junction Thermal Transport (NJTT) Program, monitored by Dr. Avi Bar Cohen, Dr. Joe Maurer and Dr. Jonathan Felbinger of DARPA. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of DARPA.